Ultrathin Indium Oxide Thin-Film Transistors With Gigahertz Operation Frequency

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***Abstract*—The remarkable dc performance of ultrathin indium oxide transistors offers a path toward high-performance back-end-of-line (BEOL) and monolithically integrated logic and memory devices for next-generation computing. Its very low thermal budget, high reliability, scalability, and 3-D conformality are additional factors that make these devices well-suited for these applications. Here, the radio frequency (RF) performance of indium oxide transistors with a high working frequency is characterized for the first time. A new record high cutoff frequency (f_T) among amorphous metal–oxide–semiconductor transistors is reported with simultaneously high maximum oscillation frequency (f_{max}). Detailed statistical measurements across a wide variety of channel lengths and gate overlaps provide insight into optimization of the device parasitics and future scaling trends. Even at relatively long channel lengths of 1 μm, the operation frequency is sufficient for these devices to function alongside traditional silicon CMOS devices that are generally clocked at less than 5 GHz.**

***Index Terms*—Atomic layer deposition (ALD), back-end-of-line (BEOL) compatible, high-frequency, indium oxide, oxide semiconductor, radio frequency (RF), thin-film transistor.**

I. Introduction

THE last several years have seen amorphous metal oxide thin-film transistors (TFTs) break past the barrier of 1 GHz operation frequency due to significant efforts in materials growth, contact optimization, device geometry, and scaling [1], [2], [3], [4], [5]. These developments enable a host of new applications, including high-speed logic and analog signal modulation in the ultrahigh-frequency (UHF) band and beyond. The disorder-resistant high mobility [6] and low thermal budget processing of amorphous metal oxides make them well-suited for back-end-of-line (BEOL) devices and monolithic 3-D (M3D) integration, which are important emerging areas of research as the silicon CMOS industry scales to single-digit nanometer nodes and chip area for peripheral circuitry becomes ever more precious [7].

Simultaneously, the last several years have revealed that extremely thin metal oxide channels can give extraordinary dc performance [4], [5], [8], [9], [10], [11], [12]. This is especially true for pure indium oxide (In_2O_3) [13], [14], [15], which has the highest mobility among its family of amorphous metal oxides. Indium oxide has been historically ignored in favor of indium–gallium–zinc oxide (IGZO) [16] and other doped relatives due to its degenerate carrier concentration and tendency to grow polycrystalline. Both of these challenges are resolved by using atomically thin layers [13]. The indium oxide channels are grown by a mature atomic layer deposition (ALD) process, which gives atomically precise thickness control, is highly uniform across arbitrary areas, and is conformal on 3-D structures [17]. The fabrication process employed has a thermal budget of 225 °C, which is fully BEOL compatible. Despite the very low thermal budget relative to traditional CMOS processing, these devices can achieve excellent on current as high as 3 A/mm in planar devices [15] and above 10 A/mm by pulsed I–V measurements [18] or with gate-all-around geometry [19], near-ideal room-temperature subthreshold swing (SS) below 70 mV/dec [14], [20], high electron mobility up to 113 $cm^2/V \cdot s$ despite being amorphous [17], I_{on}/I_{off} ratio potentially as high as 10^{17} [21], and transconductance up to 1.5 S/mm [15] (pulsed I–V: 4 S/mm [18]) in deeply scaled devices. Furthermore, the devices appear to be immune to hydrogen exposure issues that are common in BEOL materials [20], appear to be comparably stable to traditional devices under gate bias stress [22], have engineerable V_T allowing for enhancement- and depletion-mode operation [14], [20], and much like 2-D materials are resistant to short-channel effects (SCEs) due to the thin body of the channel.

However, a critical question that has not yet been addressed is that of the maximum frequency at which these devices can operate, which will play a deciding role in their available applications. This work reports for the first time the detailed RF characterization of some of these In_2O_3 transistors scaling down to 150-nm channel lengths. A high maximum oscillation frequency (f_{max}) up to 7.37 GHz and a record-level cutoff frequency (f_T) of 22.54 GHz are measured. Prescriptions for further improvement of f_T

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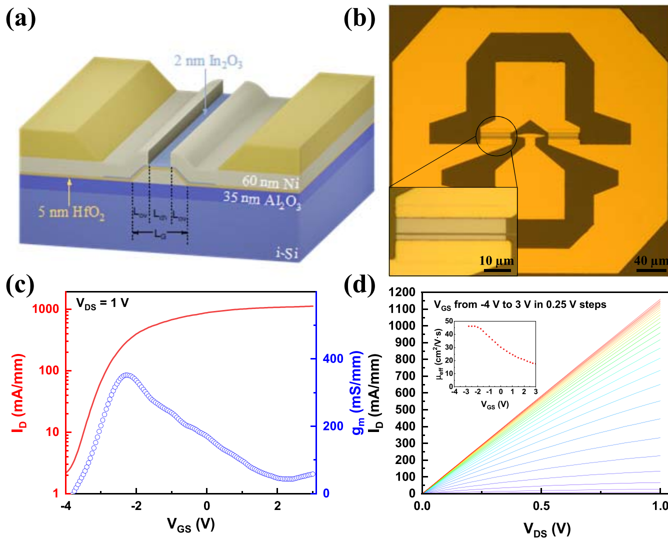

Fig. 1. (a) Illustration of the device structure studied. (b) Optical microscope image of a short-channel device with 150-nm gate length and −250-nm overlap. (Inset: channel region more clearly and the underlap can be distinguished.) The large metal pads defined by photolithography are slightly misaligned (gold color), and however, the underlying channel region is precisely aligned and defined by EBL (gray color metal). (c) Transfer characteristic with extracted g_m and (d) output characteristics for a sample device with 150-nm channel length and 100-nm overlap. (Inset: effective mobility estimated from the output curves.) The extracted field-effect mobility of this device is 36 cm^2/V·s, in good agreement. The high g_m results in good f_T, but the poor drain current saturation behavior and parasitics limit f_{max}.

and f_{max} are also discussed based on detailed statistical characterization.

II. Experiments

Devices were fabricated by a process similar to previously published work [13], [14] with a few notable exceptions. Fig. 1(a) and (b) shows a cutaway illustration and optical micrograph of the final device structure, respectively. Here, the substrate was highly resistive intrinsic silicon (>10 kΩ/□) with a coating of 35-nm Al_2O_3 grown by ALD at 175 °C with trimethylaluminum (TMA) and H_2O as the precursors. The intrinsic silicon is used to minimize substrate parasitics at high frequencies. A bilayer liftoff process is used to define the buried gate contacts by electron beam lithography (EBL). A Jeol JBX-8100FS EBL system is used to achieve high resolution and precise alignment of the contacts. SF9 (PMGI) is used as the underlayer with AR-P 6200.13 electron beam resist as the top layer. In this way, high resolution is achieved without jagged metal edges while retaining the processing simplicity of liftoff; 60-nm e-beam evaporated Ni is used for the buried gate contacts. Then, 5-nm HfO_2 grown by ALD at 200 °C using tetrakis(dimethylamido) hafnium (TDMAHf) and H_2O as the Hf and O precursors was deposited for the gate dielectric layer. A relatively thick approximately 2-nm layer of In_2O_3 was grown by ALD at 225 °C using trimethylindium (TMIn) and H_2O as the In and O precursors as the channel layer. Channel regions of indium oxide were defined by photolithography and isolated by wet etching in concentrated HCl. The source and drain contacts were defined by EBL, e-beam evaporation of 60 nm Ni, and liftoff. Gate contact windows were then photolithographically defined and the exposed HfO_2 was dry etched in an inductively coupled plasma reactive ion etching (ICP-RIE) system with BCl_3/Ar plasma. Finally, large contact pads consisting of a further 100-nm Ni/200-nm Au were photolithographically defined and deposited by e-beam evaporation. In the future, plasma treatment [14] or annealing [20] can be used to make enhancement mode RF devices. This is beyond the scope of this initial work.

Two-port scattering parameters (S-parameters) were measured using a Keysight N5225A vector network analyzer (VNA) from 30 MHz to 20 GHz in a common-source configuration with an input power of −10 dBm and an intermediate frequency (IF) filter bandwidth of 5 kHz. Form-Factor Infinity probes with 150-μm probe pitch were used to contact the device pads. Calibration to the probe tip plane was performed using short-open-load-thru (SOLT) measurements on a FormFactor impedance standard substrate. On-wafer short and open structures were employed to deembed pad parasitics from the device measurements [23]. DC biasing during RF measurement was done using Keithley 2400 SMUs connected to the VNA bias tees and synchronized programmatically [24].

f_T and f_{max} were extracted from the deembedded S-parameter measurements. For f_T, the S-parameters were converted to H parameters and the intersection of h_{21} with 0 dB was taken as f_T. For cases where f_T was greater than 20 GHz (the maximum measured frequency), h_{21} was extrapolated at a slope of −20 dB/dec.

To determine f_{max}, Mason's unilateral gain (U) was calculated directly from the deembedded S-parameters according to the following equation [25]:

$$U = \frac{|S_{21}/S_{12} - 1|^2}{2K|S_{21}/S_{12}| - 2R\{S_{21}/S_{12}\}} \tag{1}$$

where S_{ij} is the S-parameter for port i as the output port and port j as the input port and K is a stability criterion defined as follows:

$$K \equiv \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{21}S_{12}|}. \tag{2}$$

A second calculation of maximum available gain (MAG) or maximum stable gain (MSG) was performed in parallel since their 0-dB crossing also gives f_{max}.

III. Results

DC measurements of some of the In_2O_3 TFTs were collected to verify the function and identify bias points. Fig. 1(c) and (d) shows sample transfer and output characteristics for a typical device with the shortest channel length in this study of 150 nm. High g_m around 370 mS/mm and effective mobility around 47 cm^2/V·s are extracted in this device. Detailed statistical thickness-dependent dc characterization has been reported previously [13], [14], [15], [20]. Due to the thicker In_2O_3 layer without annealing or plasma treatment, compared to some of the previous work, V_T is quite negative in these RF devices and they are difficult to fully turn off [13].

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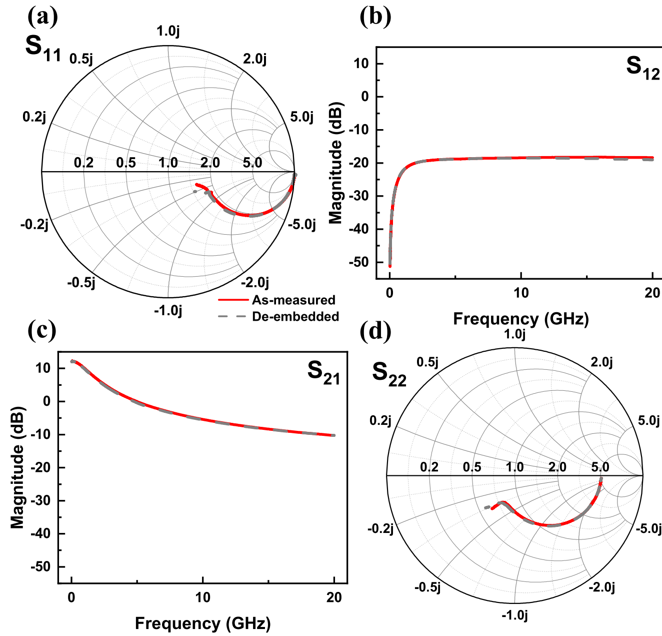

Fig. 2. Measured S-parameters of an example device with 150-nm channel length and 100-nm overlap before and after deembedding procedures. (a) S_{11}, (b) S_{12}, (c) S_{21}, and (d) S_{22}. DC biases are $V_{GS} = -2.2$ V and $V_{DS} = 1.8$ V.

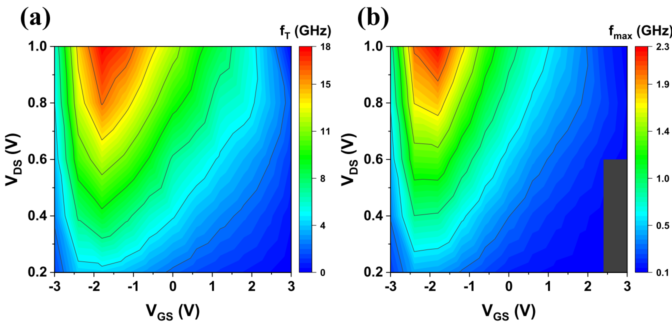

Fig. 3. Bias maps of (a) f_T and (b) f_{max} for a device with 150-nm channel length and nominally 0-nm overlap. As expected, the peaks of both f_T and f_{max} coincide with the gate bias of peak transconductance near −2 V. Short-open deembedding has been performed on these data.

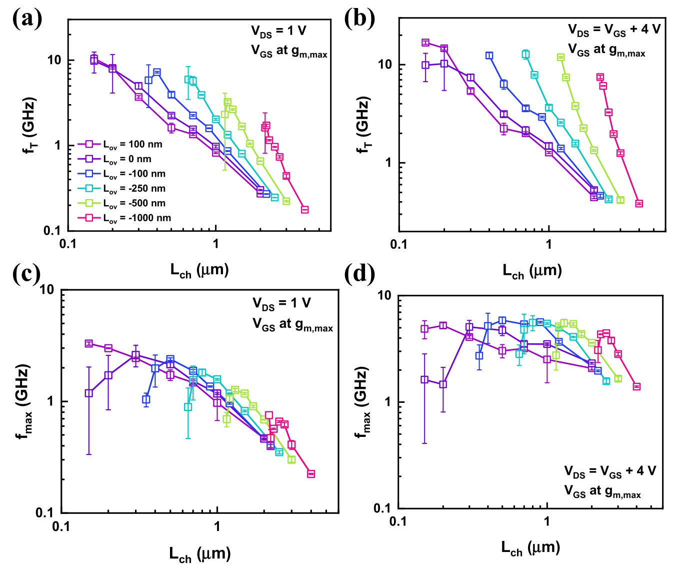

Fig. 4. Transistor (a) and (b) f_T and (c) and (d) f_{max} scaling as a function of channel length with a variety of overlap geometries. (a) and (c) constant V_{DS}. (b) and (d) devices at near maximum drain bias. The channel length is defined as the (nominal) distance from source to drain. Positive overlap indicates that the source and drain extend on top of the gate, while negative overlaps (underlaps) indicate that the source and drain have additional spacing away from the gate. Channel length, gate length, and overlap length are related by the equation $L_{ch} = L_G - 2L_{ov}$. Error bars represent the standard deviation from the average of at least five devices.

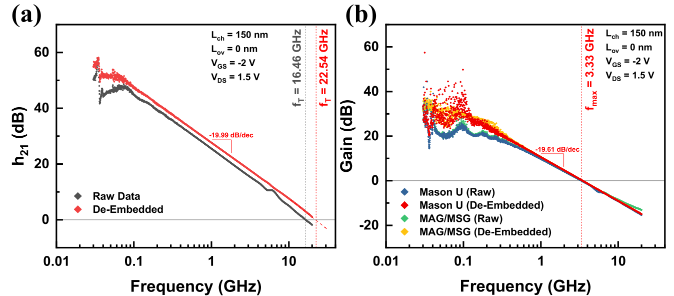

Fig. 5. Extraction of (a) f_T and (b) f_{max} for the device with the highest f_T among the measured devices. A new record f_T among amorphous metal oxide devices of 22.54 GHz is found.

The as-measured and deembedded S-parameters of a typical device are shown in Fig. 2. Since the deembedding procedure used only removes the parasitics associated with the large GSG contact pads, the difference is generally minor and is difficult to distinguish on the logarithmic scales of Fig. 2. The devices are well-behaved with large $|S_{21}|$ compared to $|S_{12}|$ indicating good forward gain.

To further optimize the dc biasing conditions, bias maps were generated for selected short channel length devices. The results are shown in Fig. 3 and clearly show that f_T and f_{max} both coincide with the point of maximum g_m as expected. Hence, the statistical study of device RF performance was conducted by biasing the gate at approximately the point of maximum g_m and biasing the drain at a constant 1 V and at V_{GS}+ 4 V, which is approximately the largest drain bias that can be applied without breaking down the gate dielectric or the channel by high current thermal effects. The latter issue can be solved by employing high thermal conductance substrates such as BN, AlN, or even diamond to improve thermal dissipation [26]. Fig. 4 summarizes the results of those measurements over a wide range of gate lengths (L_G) and overlap distances (L_{ov}). Broadly, scaling to shorter channel lengths significantly improves f_T and gives moderate improvements to f_{max} indicating that the performance does not become dominated by the contacts, consistent with our dc data. Nickel contacts to In_2O_3 have very low contact resistance (R_C) typically less than 0.1 Ω· mm and specific contact resistivity (ρ_C) less than 10^{-8}Ω· cm^2 [15], [17]. Increasing the drain bias further improves both figures of merit by increasing the transconductance, which results in the highest f_T shown in Fig. 5. The measured h_{21} and U roll-off are very near to the ideal −20 dB/dec. To the best of the authors' knowledge, this is a new record among RF amorphous metal oxide transistors [5]. Furthermore, the previous record was achieved at an

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aggressively scaled channel length of 30 nm [5], whereas the minimum channel length in this study is 150 nm. The scaling trends in Fig. 4 are optimistic for future devices with shorter gate and channel lengths. We expect to observe significant improvements to the RF performance on more scaled In_2O_3 RF transistors since performance benefits are exhibited in dc measurements when the devices are aggressively scaled down to as small as 7–8-nm channel lengths [15]. f_{max} of the reported devices is somewhat lower than f_T, which is attributed to unoptimized gate resistance and poor current saturation. The best measured f_{max} was 7.37 GHz in a device with a 200-nm gate length and −100-nm overlap.

IV. Discussion

In equivalent circuit terms, f_T and f_{max} of an MOS transistor can generally be expressed as [27]

$$f_T \approx \frac{g_m}{2\pi(C_{GS}+C_{GD})} \tag{3}$$

$$f_{max} = \frac{1}{2\sqrt{R_G}}\frac{f_T}{\sqrt{2\pi f_T C_{GD} + 1/r_0}} \tag{4}$$

where C_{GS} and C_{GD} are the gate-to-source and gate-to-drain capacitances, respectively, R_G is the gate resistance, and r_0 is the output resistance. Evaluating (3) with our typical measured dielectric capacitance (C_{ox}) value of roughly 1.5 $\mu C/cm^2$ [14] gives results in good agreement with our measured values even without accounting for fringe capacitances. One weakness of these indium oxide devices is their poor current saturation as can be seen in Fig. 1(c). As a result, the $1/r_0$ term can dominate the denominator of (4), which explains why f_{max} is low for these devices. It is possible to achieve good saturation in ultrathin indium oxide devices, but this is typically feasible at longer channel lengths for which g_m is lower. This tradeoff as well as increasing R_G with shorter gate lengths is likely the reason for the peaks in f_{max} observed in Fig. 4. Aside from that, straightforward routes to improve f_{max} are to continue scaling to shorter channel lengths (to increase f_T) or to reduce R_G. For the latter, thicker or more conductive metals can be used for the gate contact. Equation (4) predicts that reducing R_G by one order of magnitude will increase f_{max} by roughly a factor of three. Replacing the 60-nm-thick Ni buried gate contact with a slightly thicker Ag, Cu, or Au layer could accomplish this without significant design changes. Another popular method is to employ a T-gate geometry [28] in top-gated devices. Top-gated indium oxide devices are challenging due to a doping effect from the gate dielectric deposition believed to be caused by oxygen scavenging but have seen significant developments recently [26].

Fig. 6 shows the extracted $f_T \times L_G$ figure of merit for the best performing indium oxide devices in this study. The best value achieved is just over 4 GHz· μm. To the best of the authors' knowledge, this is the highest value among amorphous metal oxides. ZnO can come close to this value but has a strong tendency to grow nanocrystalline. An effective electron velocity is estimated from $f_T = v_{eff}/2\pi L_G$, which is up to 2.5 × 10^6 cm/s. This value is lower than the

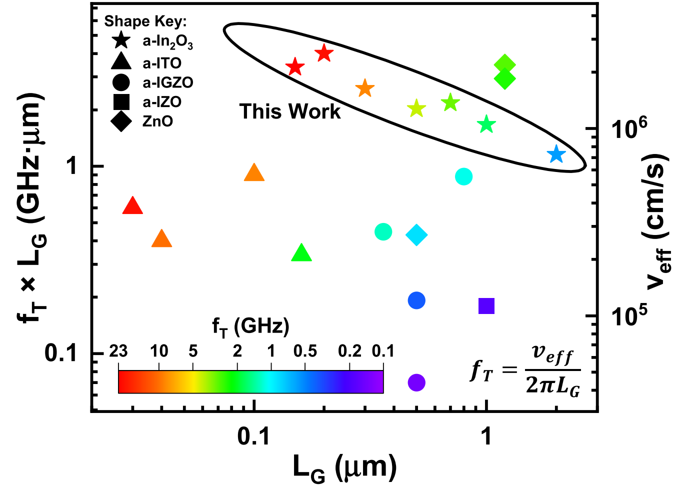

Fig. 6. Cutoff frequency times gate length for the best performing devices in the dataset and the amorphous oxide semiconductor device literature. The effective electron velocity through the device is also given. For negative overlaps, L_G is the physical length of the gate contact. For the devices with positive overlap, L_G is taken as the channel length here for the sake of comparison.

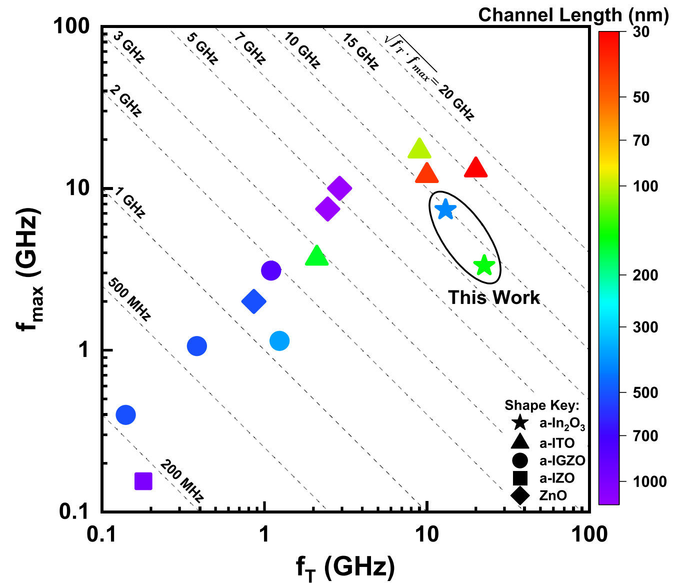

Fig. 7. Comparison to the metal oxide transistor device literature. Only wafer-scale-compatible and BEOL-compatible processes are included. Shapes correspond to channel material. Color corresponds to channel length (source to drain distance). Data points are from [1], [2], [3], [4], [5], [27], [29], [30], [31], [32], [33], and [34].

saturation velocity due to the limited drain biases applied and not accounting for resistive and capacitive parasitic delays.

Fig. 7 shows a comparison to the metal oxide RF transistor literature. Most doped indium oxides, such as IGZO, have lower mobilities that limit their g_m. Indium–tin oxide (ITO) is an exception, but in general still has lower mobility than pure indium oxide. Hence, in this work, comparable performance is achieved with pure indium oxide channels even with significantly longer gate and channel length devices. ZnO is included since it has similarities as a metal oxide channel and is noteworthy for outperforming at a given channel length. However, its strong tendency to grow nanocrystalline even in very thin layers may limit its practical usefulness due to

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reliability issues. The previous record 20 GHz f_T on ITO with a 30-nm channel length is surpassed by an unoptimized indium oxide device with a 150-nm channel length. The best $\sqrt{f_T \cdot f_{\max}}$ achieved is around 10 GHz.

V. Conclusion

High-frequency measurements of ultrathin indium oxide RF transistors have been presented from gate lengths of approximately 2 μm down to 150 nm. Record high f_T among amorphous metal oxide transistors above 20 GHz was achieved with simultaneously high $f_{\max}$. The operation speed of the devices is sufficient for them to be clocked at silicon CMOS speeds (i.e., <5 GHz) for BEOL integration. The operation frequency can be improved further by deeper channel length scaling and geometry refinement.

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